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Citation & Abstract

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

[Select All](#) [Deselect All](#)**1. Modeling architectural improvements in superscalar processors**

Zhu, Y.; Wong, W.F.;

High Performance Computing in the Asia-Pacific Region, 2000. Proceedings. The Fourth International Conference/Exhibition on

Volume 1, 14-17 May 2000 Page(s):28 - 30 vol.1

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Modeling architectural improvements in superscalar processors

[Zhu, Y.](#) [Wong, W.F.](#)

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Abstract

A model of superscalar processors using a network of Multiple-Class-Multiple-Resource queues is described and studied. The model is able to model and study instruction classes, instruction dependencies, the cache, the branch unit, the decoder unit, the instruction buffer, the functional units, the retirement buffer, the retirement unit and instruction issue policy in an integer model. The model has been verified against measured performance and has shown an average error of 5%.

Index Terms

Indexing

Controlled Indexing

[buffer storage](#) [computer architecture](#) [instruction sets](#) [performance evaluation](#) [queueing theory](#)

Non-controlled Indexing

[Multiple-Class-Multiple-Resource queues](#) [architectural improvement modeling](#) [average error](#) [branch unit](#) [central instruction buffer](#) [decoder unit](#) [functional units](#) [instruction classes](#) [instruction dependencies](#) [instruction issue policy](#) [measured performance](#) [retirement buffer](#) [retirement unit](#) [superscalar processors](#)

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